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Advanced fabrication of Si nanowire FET structures by means of a parallel approach

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Abstract

In this paper we present fabricated Si nanowires (NWs) of different dimensions with enhanced electrical characteristics. The parallel fabrication process is based on nanoimprint lithography using high-quality molds, which facilitates the realization of 50 nm-wide NW field-effect transistors (FETs). The imprint molds were fabricated by using a wet chemical anisotropic etching process. The wet chemical etch results in well-defined vertical sidewalls with edge roughness (3σ) as small as 2 nm, which is about four times better compared with the roughness usually obtained for reactive-ion etching molds. The quality of the mold was studied using atomic force microscopy and scanning electron microscopy image data. The use of the high-quality mold leads to almost 100% yield during fabrication of Si NW FETs as well as to an exceptional quality of the surfaces of the devices produced. To characterize the Si NW FETs, we used noise spectroscopy as a powerful method for evaluating device performance and the reliability of structures with nanoscale dimensions. The Hooge parameter of fabricated FET structures exhibits an average value of 1.6×10^{-3}. This value reflects the high quality of Si NW FETs fabricated by means of a parallel approach that uses a nanoimprint mold and cost-efficient technology.

Keywords: silicon nanowires, nanoimprint, roughness, noise

(Some figures may appear in colour only in the online journal)

1. Introduction

Silicon nanowire (Si NW) field effect transistor (FET) biosensors produced by using a top-down fabrication strategy have attracted much interest from researchers because of their CMOS-compatible manufacturing technique and novel properties promising the highly sensitive detection of biological molecules [1–3]. Up to now, the majority of Si NW fabrication approaches have been based on deep-UV photolithography [4] or e-beam lithography (EBL) [2]. Nanoimprint lithography (NIL), proposed in 1995 by Stephen Y Chou [5], appeared to be a competitive candidate technology for next-generation lithography [6]. As a low-cost, high-throughput and high-resolution technique for mass production, NIL has proven to be very successful in nanopatterning, especially in replicating nanoscale features [6]. In this process, the surface pattern of a nanoimprint mold is replicated into the imprint resist by mechanical deformation. The imprint resist is typically a layer of special polymer spin-coated onto the substrate. During the thermal NIL used in this work, the resist layer is heated above the glass transition temperature and then deformed by pressing through the imprint mold [7]. It should be noted that NIL neither has any diffraction limit in structure resolution, as occurs in optical lithography [8], nor suffers from the proximity effect or the charging effect seen in EBL [9].

The imprint molds (with features on the scale of tens of nanometers or smaller) are of particular interest because they can outperform modern optical lithography approaches and have much lower costs than EBL, which involves a parallel nanoscale patterning technology. Therefore, NIL is a promising technique for Si NW FET fabrication for transferring structures with features of various sizes ranging from the nanometer scale to the millimeter scale from an imprint stamp to the resist and then to the substrate by means of dry etching.

A key step in obtaining the nano-sized patterns in the resist using NIL is forming an imprint mold, which contains the nanostructures and microstructures that are to be

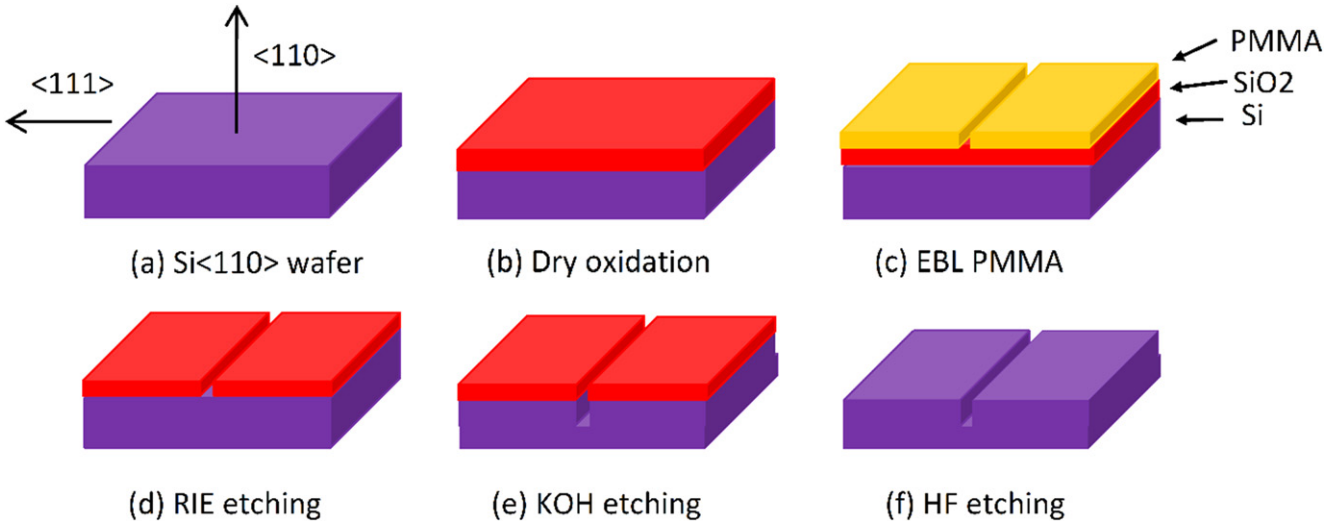

Figure 1. Schematic process of mold fabrication by using wet chemical KOH etching.

replicated simultaneously to the media. Therefore, the quality of the nanoimprint mold is crucial for success during the NIL process. In other words, the resolution of NIL is mainly limited by the resolution of the imprint mold. To date, mainly EBL and reactive ion etching (RIE) have been employed to produce NIL molds with high resolution. However, such fabrication techniques have several limitations. The first is the mold's edge roughness, which is a very important feature for NIL because it determines the quality of the replicated structure. Reducing edge roughness during EBL is time-consuming or expensive because it requires smaller beam step size and hence results in longer writing time or increasing energy of the electrons for higher resolution [10].

The second important limitation is that the vertical and smooth sidewall profile of the mold is very important in obtaining a smaller demolding force, but it is difficult to obtain exactly vertical and smooth sidewalls by using dry etching because the resist layer with edge roughness is projected onto the mold layer as well as the interaction processes with the mask layer during dry etching [11, 12]. Accordingly, there is a need to develop a technology for fabricating the NIL mold with low edge roughness and vertical sidewalls. Recently, Yu *et al* [13] presented the fabrication of nanoscale gratings with reduced line edge roughness by using nanoimprint lithography. In the present work, the NIL mold was obtained by using KOH etching because of significant differences between the etch rates of (111) planes compared with the other planes of the silicon crystal [14, 15]. However, it should be noted that the edge roughness of the vertical sidewalls was not analyzed in previous publications.

In this work, we demonstrated the fabrication of high-quality imprint molds and used them for manufacturing Si NW FETs. The quality of the NIL mold obtained by KOH wet etching was compared with one reported in the literature for the case of conventional dry etching. The results show that a NIL mold with vertical and smooth sidewalls and edge roughness of 2 nm was obtained; that value is about four times lower than obtained by traditional dry etching methods.

Table 1. The e-beam lithography parameters used for fabrication of the NIL mold.

	E-beam parameter		
Patterns	Dose (μC cm^{-2})	E-beam current (nA)	Beam step size (nm)
Conducting pads (coarse pattern)	225	150	50
Nanogrooves (fine pattern)	380	0.1	5

The Si NW FETs fabricated by using this NIL mold demonstrate improved subthreshold slope (SS) equal to 85 mV/decade. Advanced performance of the Si NW FETs has been proven by noise spectroscopy.

2. Nanoimprint mold fabrication

We fabricated the NIL mold for manufacturing Si NW FET biosensors by using a chemical etching technique. The detailed mold fabrication process is shown schematically in figure 1. A (110)-oriented Si wafer was chosen as the starting wafer (figure 1(a)). A 120 nm of SiO_2 was grown on the surface by thermal oxidation (figure 1(b)). The oxide layer served as a mask for the chemical etching of silicon. Then the negative and inverse structures were defined by e-beam lithography (Vistec EBPG 5000 Plus) in the spin-coated polymethyl methacrylate (PMMA) 669.04 resist (figure 1(c)).

The pattern with the nanogrooves was aligned to the <111> crystallographic axis of the (110) Si wafer. The Si NW FETs contain NWs and the contact regions, which are much larger than the NWs. The NWs on the NIL mold, which represent nanogrooves, were written by using fine precision. The contact areas were written by using lower precisions as a

coarse pattern. The EBL parameters used for coarse and fine patterns are listed in Table 1.

Reactive ion etching was then used to transfer the structure to the SiO_2 layer (figure 1(d)) by means of CHF_3 plasma (gas flow 20 sccm, power 200 W, bias −466 V). After stripping the PMMA resist, the sample was dipped into a 20% KOH solution at 30 °C [16, 17] (figure 1(e)). Both these parameters ensure a small etching rate, which results in better surface quality. Before submerging the mold into the KOH solution bath, the native SiO_2 was removed by using 1% HF etching for 20 s. As mentioned previously, the SiO_2 pattern was used as an etching mask to etch the (110) Si layer by means of anisotropic wet etching. The etching rate of crystalline silicon in the (111) is much slower than that in the (110) planes; therefore, anisotropic chemical etching allows a Si nanogroove to be obtained with two vertical sidewalls of (111) planes with nearly atomic scale smoothness, even if the original SiO_2 etch mask has serious edge roughness created by EBL and the Si nanogroove was projected onto the SiO_2 layer by dry etching.

After KOH etching, the sample was dipped into buffered hydrofluoric acid (BHF) solutions to remove the SiO_2 mask layer (figure 1(f)).

3. Results and discussion

3.1. SEM and AFM characterization of mold quality

The quality of the molds was characterized by scanning electron microscopy (SEM) and atomic force microscopy (AFM). The SEM image of an imprint mold fabricated by using KOH chemical etching is shown in figure 2(a). As can be seen from the image, two kinds of structures are combined in the fabricated mold: the micron-scale contact lines and the nanogrooves (the height of which is about 220 nm), representing Si NW. The red square indicates one of the nanogrooves in figure 2(a). The structure was cut by fusing focused ion beam (FIB). The SEM image of the FIB cut of the nanogroove is shown in figure 2(b).

The quality of the nanogroove sidewalls is crucially important for further device fabrication processes. Figure 2(b) demonstrates that after anisotropic chemical wet etching, we obtain vertical sidewalls along the (111) planes as a result of chemical anisotropic etching in an aqueous KOH solution, which provides a high ratio of about 200:1 between the etch rates of the (110) to (111) planes of the Si crystal [14]. The 3D and 2D AFM images of the single nanogroove of the fabricated imprint mold are shown in figures 2(c) and (d). The measured depth of the mold is about 220 nm.

To investigate Si nanogroove etching along different orientations of the Si wafer, we designed test structures within the mold with nanogroove arrays along two directions. Figures 3(a) and (b) show the results of etching the nanogroove arrays oriented perpendicular to the <111> direction. As can be seen, the etching occurs along the (111) plane (the (110) plane is on the top surface). The inset of figure 3(a) shows the FIB cross section of the nanogroove arrays. It reflects the quality of the fabricated trenches. The layer on top of the mold in the inset is platinum to preserve the structure of the mold during FIB cutting. Figures 3(c) and (d) show the results of etched nanogroove arrays. These arrays were oriented along the <111> direction, which is perpendicular to the (111) planes. Therefore, the etched nanogrooves have coarse and sloped planes. These results further confirm that the chemical etching procedure used is highly anisotropic.

The molds were further analyzed by using AFM and SEM images with regard to the features of height (h), surface roughness (root mean square, r/RMS), width (w), and edge roughness (3σ) and compared with the results of the mold fabricated by means of the traditional dry etching technique used in [18]. In [18], PMMA was used as a positive resist and the structures were transferred into a polysilicon layer by RIE with HBr, which also provides anisotropic etching [19]. A silicon nitride layer underneath the polysilicon was used as an etch stop.

Table 2 shows a comparison of the height (h), surface roughness (root mean square, r), width (w,) and edge roughness (3σ) obtained from AFM and SEM images of nanoimprint molds fabricated by using the traditional dry etching method [18] and KOH chemical etching. It should be noted that the data for table 2 were obtained from an analysis of the nanoimprint mold fabricated by using wet chemical etching with a depth of 220 nm. The widths of the fabricated nanogrooves are 125, 135, and 320 nm. Two representative SEM images of this mold are shown in figures 3(a) and (b) at different magnifications. All of the measured structures have an edge roughness (3σ) of about 2 nm. Analyzing the data from table 2, we can conclude that the edge roughness of nanoimprint molds obtained by wet chemical etching is about four times lower than for molds fabricated by dry etching techniques.

The top surface of the chemically etched mold has a very small surface roughness (RMS) of 1.5 nm, which is smaller than the roughness obtained after dry etching. The RMS of the bottom of the chemically etched mold is 2.5 nm, which is higher than the value measured at the top surface of the mold, which is not exposed to the KOH etching solution because it is protected by the oxide mask. The roughness of the top surface is determined by the initial roughness of the silicon surface and the quality of the thermal oxide mask.

The bottom layer of the mold is etched by the KOH solutions and its RMS was mainly caused by random masking of the silicon surface by the H_2 bubbles produced in the reaction during the chemical etching process [20]. Adding isopropyl alcohol (IPA) may reduce this effect and thus improve the value of surface roughness [21, 22]. Another possible solution is the introduction of a high-quality etch stop layer, such as buried oxide in the silicon-on-insulator (SOI).

3.2. Si NW FETs fabricated by using developed mold

Silicon nanowire FET biosensors were fabricated by using thermal nanoimprint lithography [23] and the mold fabricated by chemical wet etching. Figure 4(a) shows the Si NW FET with the SiO_2 and Al_2O_3 stack as the gate dielectric layer, and

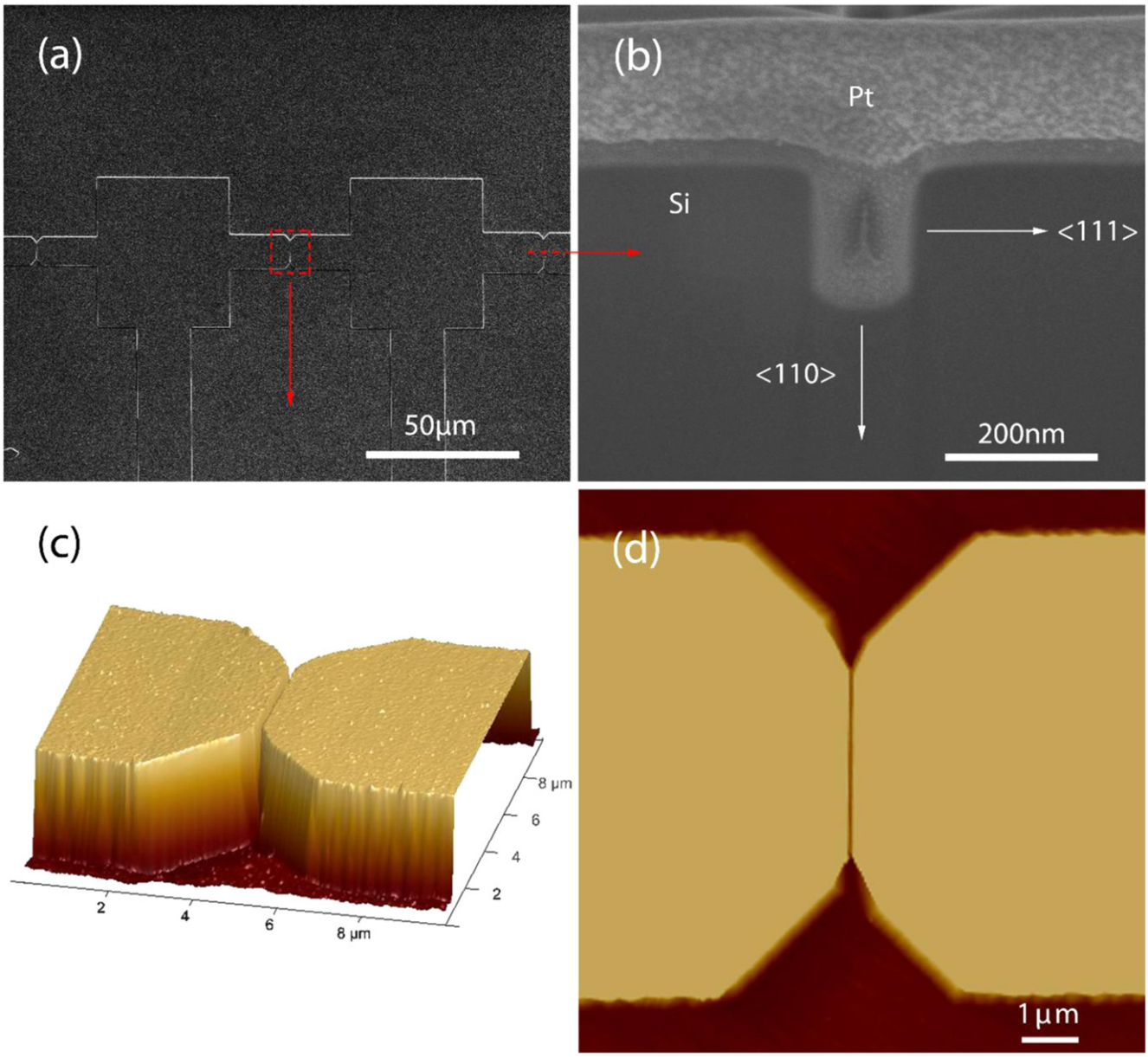

Figure 2. Surface characterizations of an imprint mold fabricated by using KOH etching: (a) SEM image of a mold. The red square indicates a single nanogroove. (b) FIB cross section of the nanogroove of the mold. Dimensions of nanogroove cross section: height 220 nm, width 135 nm. 3D (c) and 2D (d) AFM images of the nanogroove in the fabricated imprint mold.

the inset shows the amplified NW with a width of about 50 nm. This demonstrates that high-quality NW structures with a characteristic size of 50 nm and even smaller can be obtained by using thermal nanoimprint lithography.

The *I-V* characteristics of the obtained structures were measured. The transfer curves of the Si NW device with an NW width of 250 nm and length of 5 μm are shown in figure 4(a). The front gate voltage (V_{FG}) was applied through an electrochemical reference electrode immersed in the electrolyte solution (PBS (0.01 mM), pH 7.4).The back gate was floated during these measurements, the V_{FG} was swept from 1.5 V to −2 V, and the drain source voltage (V_{DS}) was varied from −0.1 V to −1.1 V in steps of −0.2 V. The produced Si NW FETs expressed p channel depletion transistors and have a threshold voltage (V_{Th}) of about 0.7 V. The subthreshold slope extracted from the transfer-characteristic curve in the logarithmic scale is 85 mV/decade; the I_{on}/I_{off} ratio reaches 10^5 at $V_{DS} = -0.1$ V. These values are comparable to the values from the reported literature and indicate a low gate dielectric trap density and good performance [24, 25].

To compare the noise level of our devices with noise values reported in the literature, we estimated the Hooge parameters by using Hooge's empirical model of *1/f* noise [26]:

$$\frac{S_I}{I_D^2} = \frac{\alpha_H}{fN} \tag{1}$$

where S_I is the drain current spectral density, N is the number of carriers, and α_H is Hooge's parameter, which is

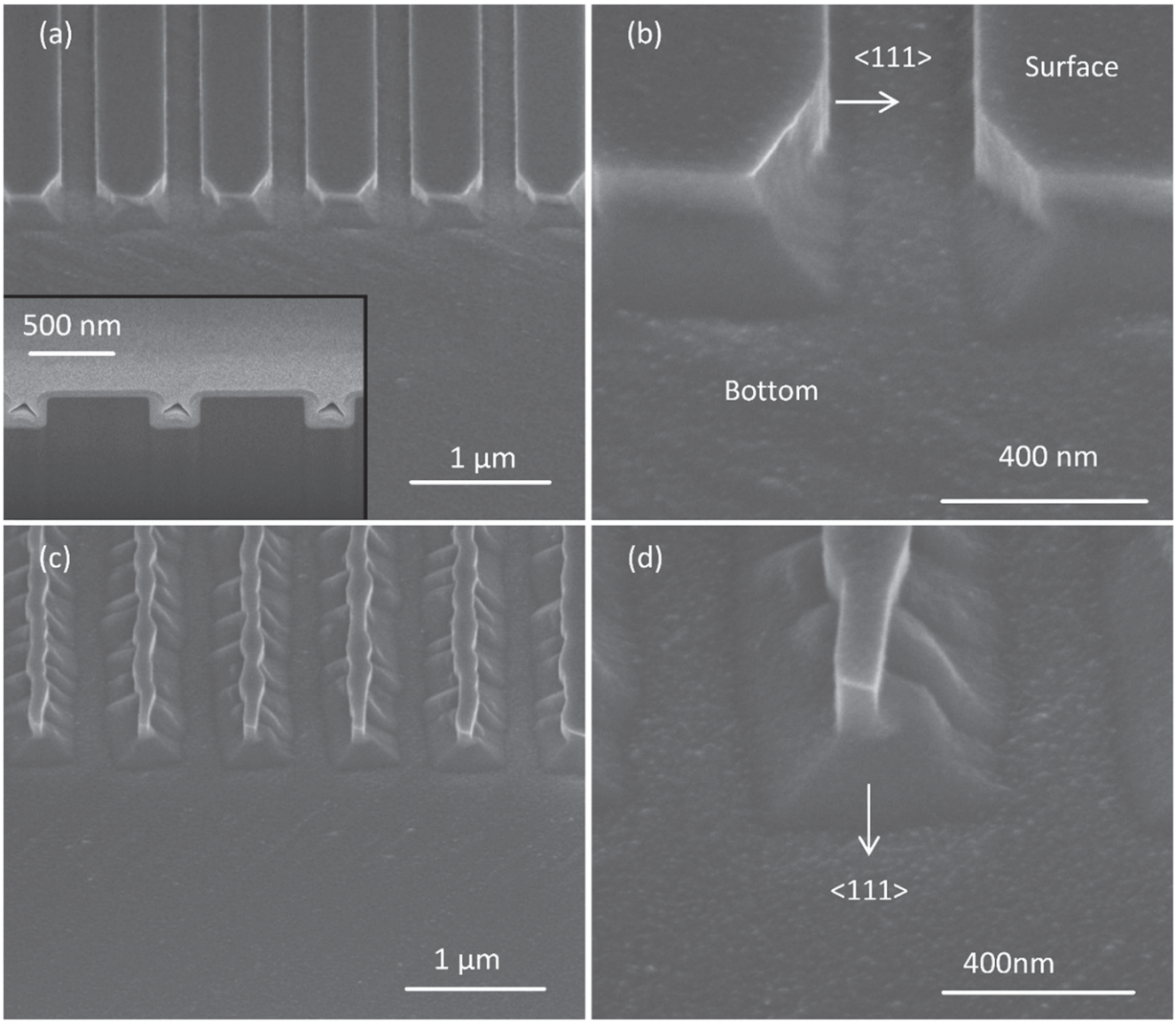

Figure 3. SEM image of a nanoimprint mold with nanogroove arrays along different directions fabricated by using KOH etching: (a) SEM image of nanogroove arrays aligned along (111) planes. The inset shows the FIB cross section of the obtained mold. (b) Zoomed single nanogroove from the SEM image of (a). (c) SEM image of nanogroove arrays aligned perpendicular to (111) planes. (d) Magnified SEM image from (c).

Table 2. Parameters of molds fabricated by using RIE and KOH etching.

		Roughness, r nm^{-1}				
Molds	Height, h nm^{-1}	Surface	Bottom	Edge roughness, w(3σ)/nm		
RIE etching [18]	107	2	n/a	94(8)	75(6)	66(7)
KOH etching	220	1.5	2.5	125(2)	135(2)	320(1.5)

dimensionless and is usually used to quantitatively assess and compare the noise performance of various devices. The number of carriers is calculated by using the drain current I_D of the transistor. The drain current follows Ohm's law in the linear regime. Drain current density can be expressed as follows:

$$I_D = nq\mu EWh \tag{2}$$

where q is the elementary charge, E is the electric field, n, and μ is the concentration of carriers in the conducting channel of

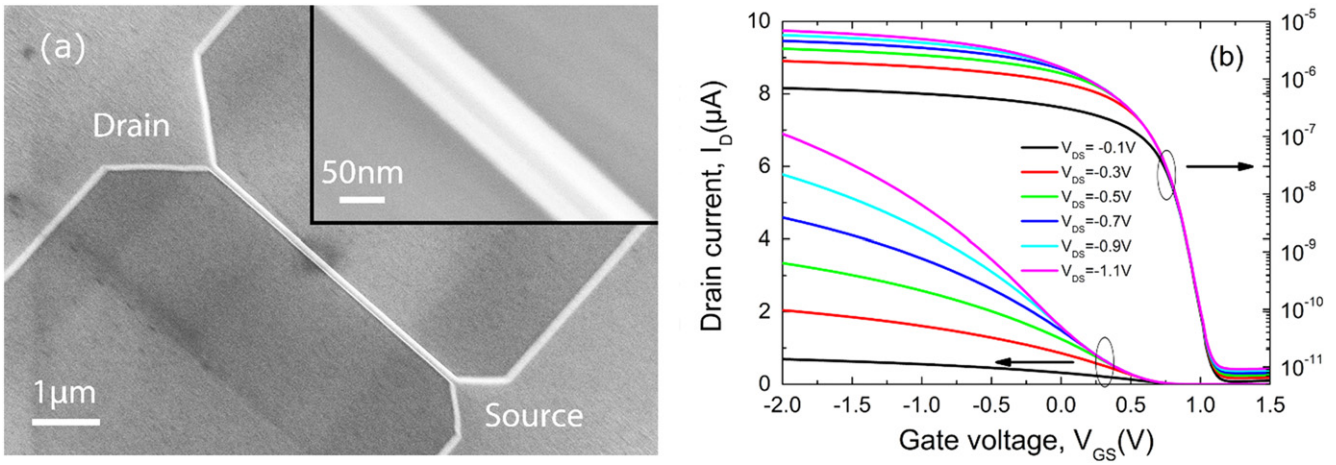

Figure 4. (a) SEM image of Si NW FET with drain, source, and NW channel. The inset shows the amplified NW section. (b) Transfer characteristic of Si NW FET biosensor with width = 250 nm and length = 5 μm on a linear and logarithmic scale.

the NW FET and carrier mobility, respectively. The concentration can be expressed as N/V, where N is the total number of carriers and $V = W \times L \times h$ is the volume of the NW channel. Here W is the width of the NW channel, h is the heigth, and L is the length channel. E equals V_{DS}/L.

The effective mobility μ of the NW FETs can be estimated by using the following equation for long-channel FETs at low drain-source voltage from the equation given in [27, 28]

$$\mu = \frac{L g_m}{W C_{ox} V_{DS}} \tag{3}$$

where $C_{ox} = \varepsilon_r \varepsilon_0 / t$ is the gate capacitance, g_m is the maximum transconductance obtained from the transfer characteristics, L is the transistor channel length, W is the width of the channel, V_{DS} is the drain source voltage, ε_r is the dielectric constant of SiO_2, and t is the thickness of the SiO_2 layer. Using $\varepsilon_r = 3.9$, $t = 9.8$ nm, $V_{DS} = 100$ mV, we obtain the mobility, which is on average about 130 $cm^2\,V^{-1}\,s^{-1}$ and is comparable with the reported results [2] for p channel Si NW FET biosensors. Thus we can calculate the total number of carriers, N, at the point of the maximum transconductance of the transfer curve by using the following equation [29–31]:

$$N = \frac{I_D L^2}{q V_{DS} \mu} \tag{4}$$

Then, according to the equation (1) Hooge's parameter, α_H, can be expressed as [31, 32]:

$$\alpha_H = \frac{f S_I}{I_D} \cdot \frac{L^2}{q V_{DS} \mu} \tag{5}$$

The value obtained for Hooge's parameter is shown in figure 5 for different lengths of the NW FET. The Hooge parameter exhibits a minimum value of 6.9×10^{-4} and an average value of 1.6×10^{-3}, which is lower than values reported for traditional EBL-processed samples [28].

The low values of Hooge's parameters also reflect the high quality of the surfaces of the fabricated Si NW FETs.

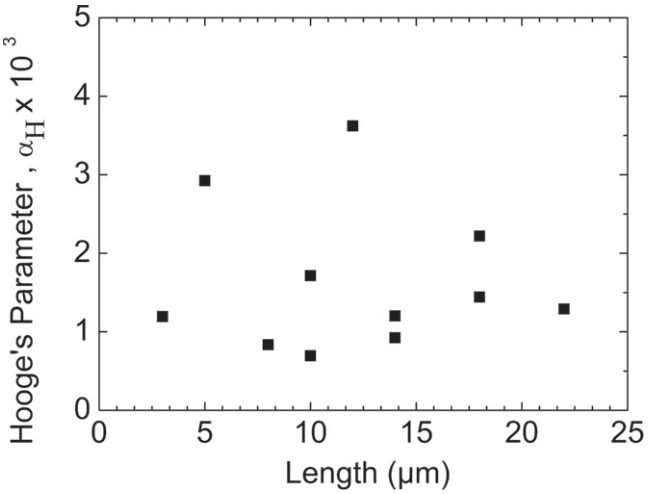

Figure 5. Hooge's parameter, obtained for Si NW FETs with 250 nm nanowire width and different channel lengths. The NW length ranges from 3 μm to 22 μm.

4. Conclusion

In summary, we fabricated advanced silicon NW structures by using a KOH wet-etched nanoimprint mold with decreased roughness. The quality of the produced mold was verified by using SEM and AFM images. It was shown that the edge roughness of the vertical sidewalls of the nanoimprint mold produced by using KOH etching is four times lower than the edge roughness obtained by using a conventional dry etching approach.

The fabricated nanoimprint mold has the advantages of vertical sidewalls with edge roughness of 2 nm and improved surface roughness of 1.5 nm. The mold was used to produce fully functional, high-quality Si NW FETs with different NW sizes and feature sizes ranging from tens of micrometers down to a few tens of nanometers. The fabricated structures were studied by using noise spectroscopy. The Hooge's parameter obtained is on the order of 1×10^{-3}, which is lower

than that reported for traditional fabrication technologies. This value is even comparable to or lower than the values reported for Si NW FET produced by EBL.

Chemical etching is a promising technique which may replace dry etching for NIL mold fabrication since it offers higher-quality molds for the fabrication of different device structures, which may scale down to the nanometer range.

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